High Density Feasibility Study

Objectives (preliminary)

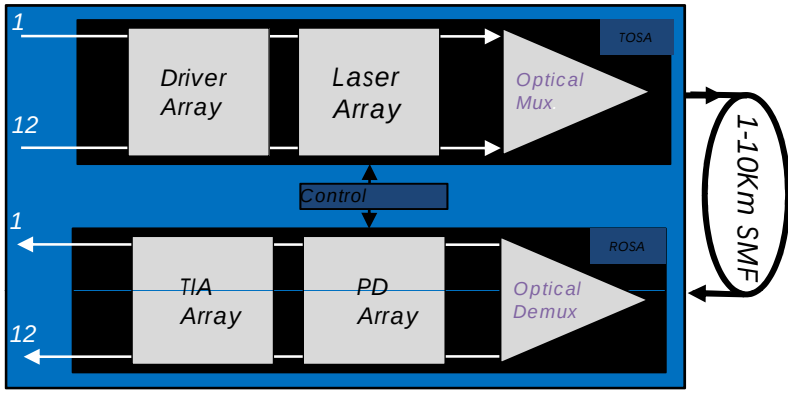
- 100G over 2Km SMF
- Backward Compatible
  - Centered at 1550nm
  - 8nm spacing
- Max power 6W
- Support OTN rate
- Support for longer reach optional

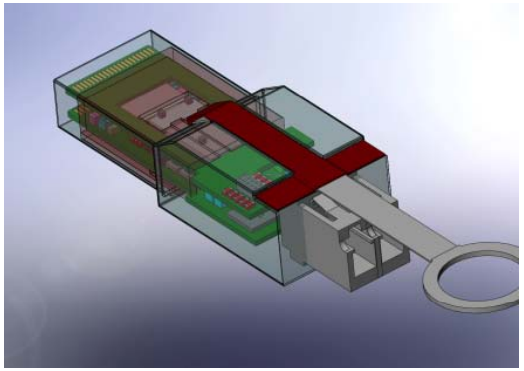
Scope

- Max 8 modules per faceplate
- Max 10Km reach
- Optional features
  - Up to 12 lanes
  - Higher rate per lane
- CXP or CXP-like form factor
  - Preference for re-use

Overview

- Based on Proven 12x10G Array architecture
  - TX: DFB and driver array with mux
  - RX: PD and TIA array with demux
- CXP host interface, no CDR
- CXP EF connector solution
  - Optional new pin field
- Dual LC receptacle
- Interoperable with LR10 CFP
- Novel optical engine design optimized for thermal management





Focus is on building small, low cost, low power optical engines
Form factor decision assigned to MSA

Thermal and Signal integrity

- Thermal solutions
  - Direct attach heat source to module cover
  - Side by side vs. stacked OSAs

- Signal integrity solutions
  - Optimized pin field
  - Improved CXP connector
  - Improved routing internal to module

Next Steps

- Thermal modeling based on form factors
  - Using new design concept
  - Working with system designers for optimal solution

- Power dissipation break down

- Signal integrity simulations based on new internal routing

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